Update on the SVX4 chip for CDF/D0

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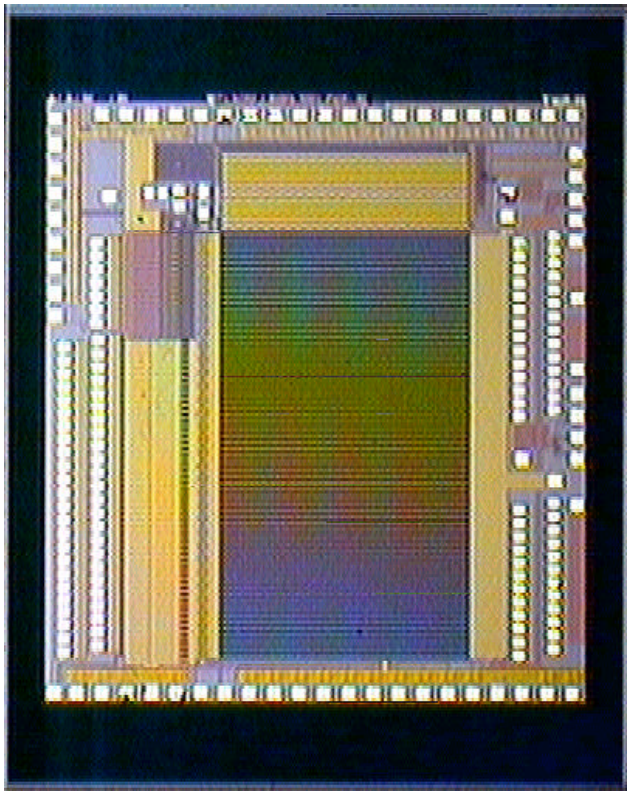
Introduction

- Tremendous progress from a year ago
  - Every indication that a fully functional full size chip will be submitted by the end of the year. Project schedule risk of a time scale of order ~ a year is now measured in a ~ couple of months.
- A single chip used by both experiments is almost a certainty
  - Recent progress defining the pad frame
  - No known serious technical issues
- Beginnings of the next stages are happening
  - Testing: wafer scale, bench characterization, etc.
  - Hybrid designs and mechanical layouts

SVX4FE Test chip



Classic case of why you build test chips:

-thinned and not plated

-struggle to make low R contact to backside

-wrong process (non-epi vs epi) => substrate is not low R anyway

-parts sent to Accurel

-Design rule files were ambiguous and not complete. Some re-design of the pipeline is necessary. (Yield is 13/37 w/o shorts)

Measurements

- Tom has made measurements on a SVX4FE chip w/o shorts.
  - It works (both preamps and pipeline)!
  - Compare FNAL/LBNL preamps

From Tom's note on his initial test results:

There are several areas of concern with the version A preamp:

1. The risetime is very dependent on the preamp output level.
2. The BW bits do not step the risetime in desirable increments. (I think 1 and 2 are related to the BW switch size used).
3. The input transistor length of 0.46u is too short – excess noise. Could be very process/run dependent. (DXL = ± 0.025μ)
4. The preamp reset rings and takes a considerable amount of time, especially if the accumulated preamp charge is big and the BW caps are switched in.
5. AVDD rejection is poor.
6. The preamp gain changes as a function of the preamp output level. This is only about a 1% effect on the test chip, but will depend on process variations, etc.

Measurements

First, compare a noise measurement made directly at the preamp output with a noise measurement made at the pipeline output (correlated double sampling).

Noise measurement directly at preamp output through a high pass filter (Version B):

50 us filter: 1.62 mV rms
5 us filter: 1.51 mV rms

At the pipeline output (pipe gain = 3.53):

100 ns sampling: 6.7 mV rms
>> 100 ns sampling: ~ 8 mV rms

Intuitive conclusion: Pipeline sampling attenuates low frequency noise but multiplies white noise by root 2.

Summary of preamp noise measurements made at pipeline output (100 ns sampling, 70 ns preamp risetime, 250 uA bias):

Version	Input W/L	Noise
A	1600/0.46	420e + 47.8 e/pF
B1	1600/0.4	400e + 58.0 e/pF
B2	1600/0.6	420e + 46.3 e/pF
B3	1600/0.8	450e + 43.0 e/pF
B4	1200/0.4	360e + 62.3 e/pF
B5	1200/0.6	330e + 51.7 e/pF
B6	1200/0.8	410e + 45.0 e/pF
B7	800/0.8	360e + 53.0 e/pF

Noise is similar for both preamps

Conclusion: For channel length < 0.8u, gm increases but there is an excess noise contribution, which becomes significantly larger around 0.4u length. For large input capacitance (40-50 pF), 1600/0.8 is close to the optimum input W/L.

Open Issues

- Decide upon which preamp to use
- FNAL has offered to take responsibility of the entire front-end (FNAL preamp, pipeline, black hole clamping, etc.)
- Finalize additional features
  - Programmable Vcal
  - Anything else
- Two chips or one?
  - Some concern over on chip bypassing
  - Test any other features?

Back-end and integration

- Minimal discussion at Wednesday meetings (to be corrected with updates from LBNL to FNAL).
- Design, layout, and post layout simulation completed on:
  - FIFO
  - Counter
  - I/O
  - ADC
- Lots of integration work remains.
- Schedule has slipped by ~2 months from the last published schedule
- Review (at FNAL?) in October